



POSEICO SPA
Power SEMiconductors Italian Corporation

POSEICO SPA
Via N. Lorenzi 8, 16152 Genova - ITALY
Tel. +39 010 6556234 - Fax +39 010 6557519
Sales Office:
Tel. +39 010 6556775 - Fax +39 010 6442510

HIGH CURRENT PHASE CONTROL THYRISTOR INSULATED MODULE

- Full hermetic packaging
- Base plate insulation using AlN substrate
- Industrial compatible packaging
- Contract screws available on request

AZT800

Repetitive voltage up to **1800 V**
Mean on-state current **800 A**
Surge current **30 kA**

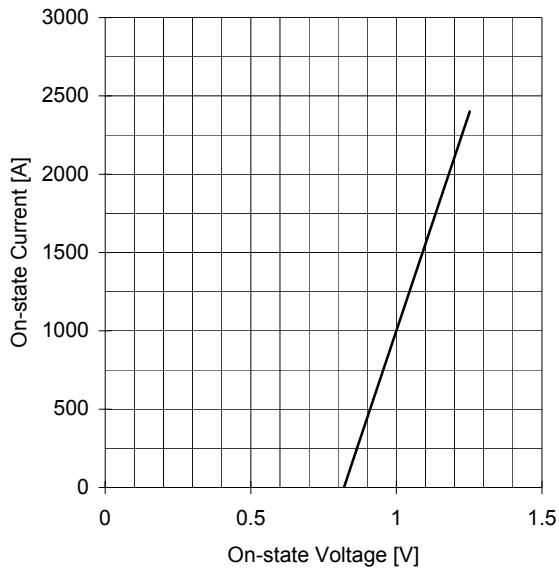
TARGET SPECIFICATION

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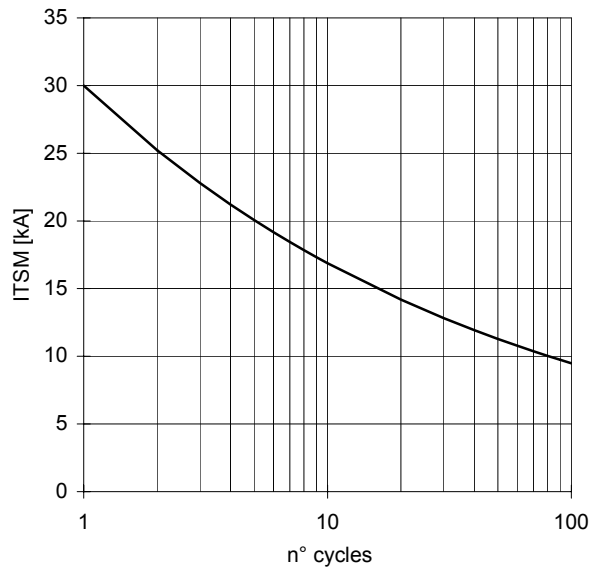
| Symbol | Characteristic | Conditions | T _j [°C] | Value | Unit |
|--|--|--|------------------------|-----------|------------------|
| BLOCKING | | | | | |
| V _{RRM / DRM} | Repetitive peak reverse/off-state voltage | | 125 | 1800 | V |
| V _{RSM} | Non-repetitive peak reverse voltage | | 125 | 1900 | V |
| I _{RRM / DRM} | Repetitive peak reverse/off-state current | | 125 | 70 | mA |
| CONDUCTING | | | | | |
| I _{T (AV)} | Mean on-state current | 180° sin, 50Hz, T _c =85°C | | 800 | A |
| I _{T (AV)} | Mean on-state current | 180° sin. 50Hz, T _c =55°C | | 1220 | A |
| I _{TSM} | Surge on-state current | sine wave, 10 ms | 125 | 30 | kA |
| I ² t | I ² t | without reverse voltage | | 4500 x1E3 | A ² s |
| V _T | On-state voltage | On-state current = 1800 A | 25 | 1.34 | V |
| V _{T(TO)} | Threshold voltage | | 125 | 0.82 | V |
| r _T | On-state slope resistance | | 125 | 0.180 | mohm |
| SWITCHING | | | | | |
| di/dt | Critical rate of rise of on-state current, min. | From 75% V _{DRM} up to 1050 A, gate 10V 5 ohm | 125 | 200 | A/μs |
| dv/dt | Critical rate of rise of off-state voltage, min. | Linear ramp up to 70% of V _{DRM} | 125 | 500 | V/μs |
| t _d | Gate controlled delay time, typical | V _D = 100V, gate source 25 V, 10 ohm, t _r = 0.5 μs | 25 | 3 | μs |
| t _q | Circuit commutated turn-off time, typical | dV/dt = 20 V/μs linear up to 75% V _{DRM} | | 250 | μs |
| Q _{rr} | Reverse recovery charge | di/dt = -20 A/μs, I = 700 A | 125 | | μC |
| I _{rr} | Peak reverse recovery current | V _R = 50 V | | | A |
| I _H | Holding current, typical | V _D = 5V, gate open circuit | 25 | 300 | mA |
| I _L | Latching current, typical | V _D = 5 V, t _p = 30 μs | 25 | 700 | mA |
| GATE | | | | | |
| V _{GT} | Gate trigger voltage | V _D = 5 V | 25 | 3.5 | V |
| I _{GT} | Gate trigger current | V _D = 5 V | 25 | 300 | mA |
| V _{GD} | Non-trigger gate voltage, min. | V _D = V _{DRM} | 125 | 0.25 | V |
| V _{FGM} | Peak gate voltage (forward) | | | 30 | V |
| I _{FGM} | Peak gate current | | | 10 | A |
| V _{RGM} | Peak gate voltage (reverse) | | | 5 | V |
| P _{GM} | Peak gate power dissipation | Pulse width 100 μs | | 150 | W |
| P _G | Average gate power dissipation | | | 2 | W |
| MOUNTING | | | | | |
| R _{th(j-c)} | Thermal impedance, DC | Junction to case | | 42 | °C/kW |
| R _{th(c-h)} | Thermal impedance | Case to heatsink | | 20 | °C/kW |
| T _j | Operating junction temperature | | | -30 / 125 | °C |
| V _{ins} | RMS insulation voltage | 50Hz, circuit to base, all terminal shorted | 25 | 4500 | V |
| T | Mounting torque | Case to heatsink | | 4 to 6 | Nm |
| | Mass | | | 2800 | g |
| ORDERING INFORMATION : AZT800 S 18 | | | | | |
| standard specification <input type="checkbox"/> <input type="checkbox"/> VDRM&VRRM/100 | | | | | |

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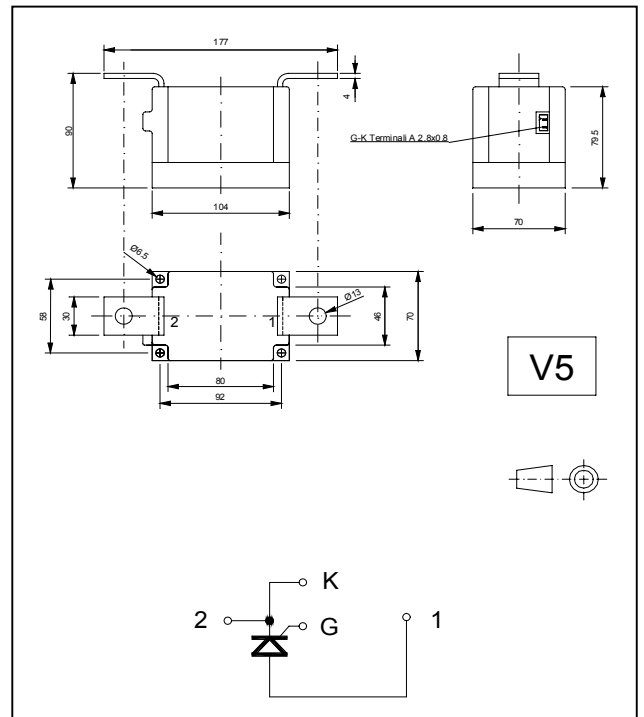
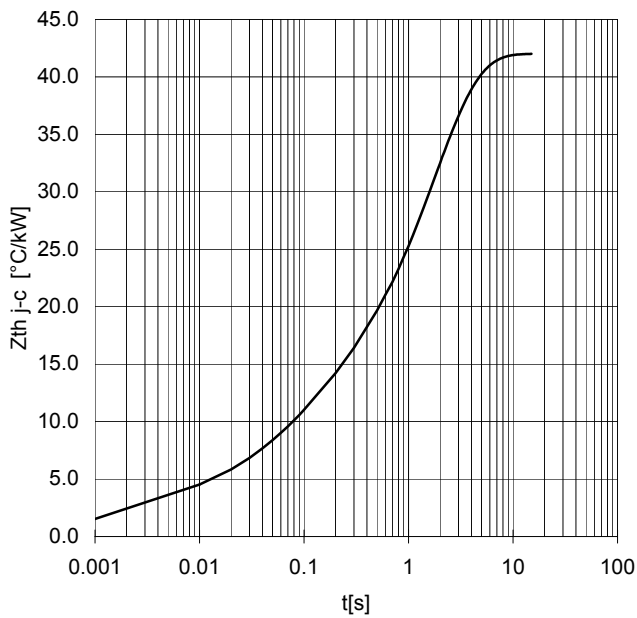
ON-STATE CHARACTERISTIC
T_j = 125 °C



SURGE CHARACTERISTIC
T_j = 125 °C



TRANSIENT THERMAL IMPEDANCE



All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.
In the interest of product improvement POSEICO SPA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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