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Power SEmiconductors Italian Corporation

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PHASE CONTROL MODULE

ATD571, ADT571

- *Full ermetic packaging
- *Industrial compatible packaging
- *Insulation using Aln substrate
- *New G-K auxiliary output arrangement
- *Contact screws available on request

Repetitive voltage up to **1600 V**
Mean on-state current **570 A**
Surge current **14.5 kA**

FINAL SPECIFICATION

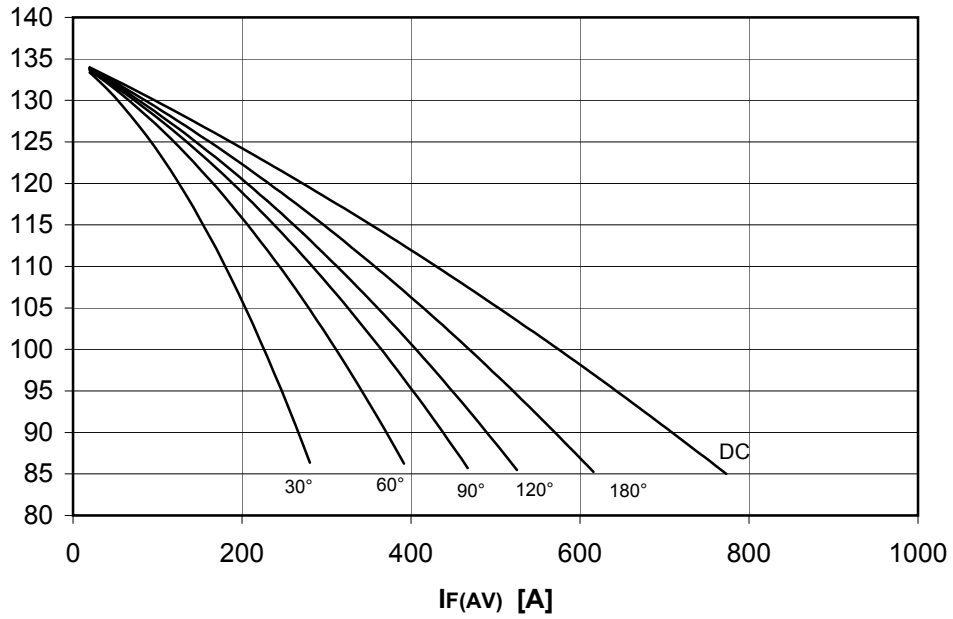
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Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM / DRM}	Repetitive peak reverse/off-state voltage		135	1600	V
V _{RSM}	Non-repetitive peak reverse voltage		135	1700	V
I _{RRM / DRM}	Repetitive peak reverse/off-state current		135	50	mA
CONDUCTING					
I _{T(AV)}	Mean on-state current	180° sin, 50Hz, T _c =91°C		570	A
I _{T(AV)}	Mean on-state current	180° sin. 50Hz, T _c =55°C		875	A
I _{TSM}	Surge on-state current	sine wave, 10 ms	135	14.5	kA
I ² t	I ² t	without reverse voltage		1051 x1E3	A ² s
V _T	On-state voltage	On-state current = 1600 A	25	1.63	V
V _{T(TO)}	Threshold voltage		135	1.0	V
r _T	On-state slope resistance		135	0.380	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% V _{DRM} up to 1050 A, gate 10V 5ohm	135	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V _{DRM}	135	500	V/μs
t _d	Gate controlled delay time, typical	VD=100V, gate source 25V, 10 ohm , tr=.5 μs	25	1.1	μs
t _q	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V _{DRM}		200	μs
Q _{rr}	Reverse recovery charge	di/dt=-20 A/μs, I= 700 A	135		μC
I _{rr}	Peak reverse recovery current	VR= 50 V			A
I _H	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I _L	Latching current, typical	VD=5V, tp=30μs	25	700	mA
GATE					
V _{GT}	Gate trigger voltage	VD=5V	25	3.5	V
I _{GT}	Gate trigger current	VD=5V	25	250	mA
V _{GD}	Non-trigger gate voltage, min.	VD=V _{DRM}	135	0.25	V
V _{FGM}	Peak gate voltage (forward)			30	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			5	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		150	W
P _G	Average gate power dissipation			2	W
MOUNTING					
R _{th(j-c)}	Thermal impedance	Junction to case, per element		50	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, per element		20	°C/kW
T _j	Operating junction temperature			-30 / 135	°C
V _{ins}	RMS insulation voltage	50Hz, circuit to base,all terminal shorted	25	4500	V
T	Mounting torque	Case to heatsink		4 to 6	Nm
		Busbars to terminals		12 to 18	Nm
	Mass			1500	g
ORDERING INFORMATION : ATD571, ADT571 S 16					
standard specification <input type="checkbox"/> <input type="checkbox"/> VDRM&VRRM/100					

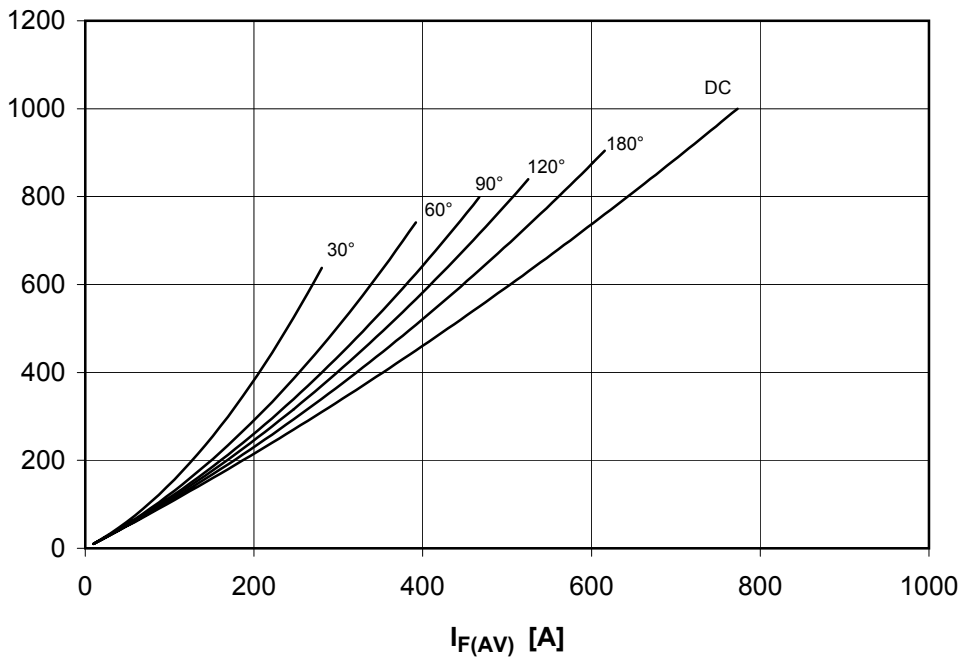
DISSIPATION CHARACTERISTICS

SQUARE WAVE

T_{case} [°C]



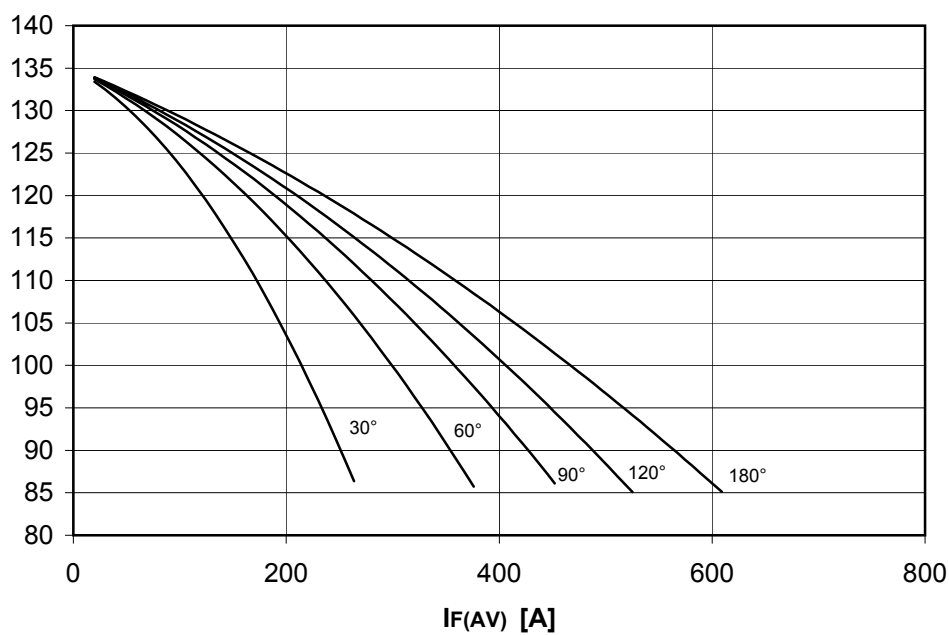
P_{F(AV)} [W]



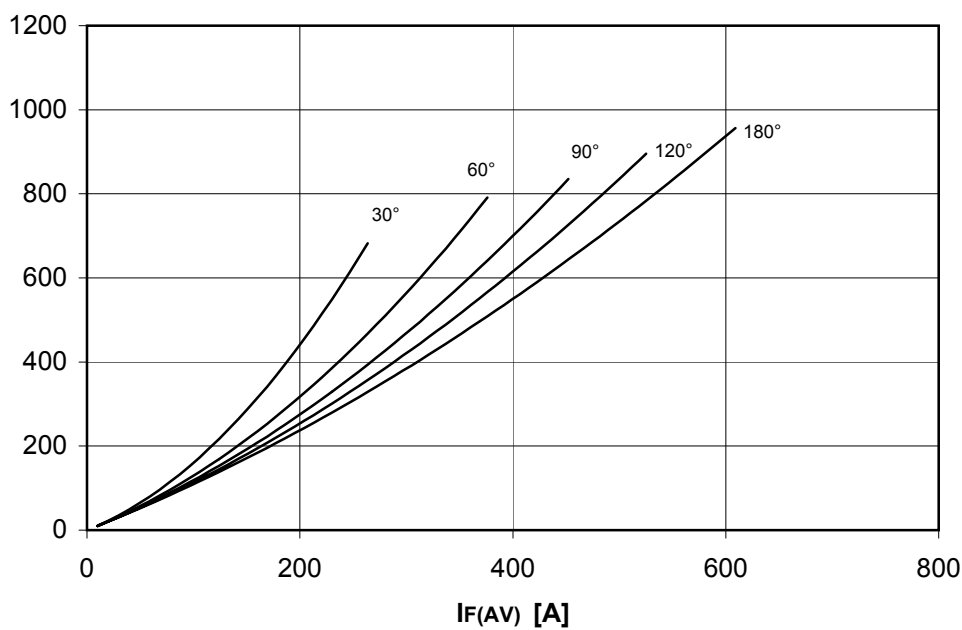
DISSIPATION CHARACTERISTICS

SINE WAVE

T_{case} [°C]



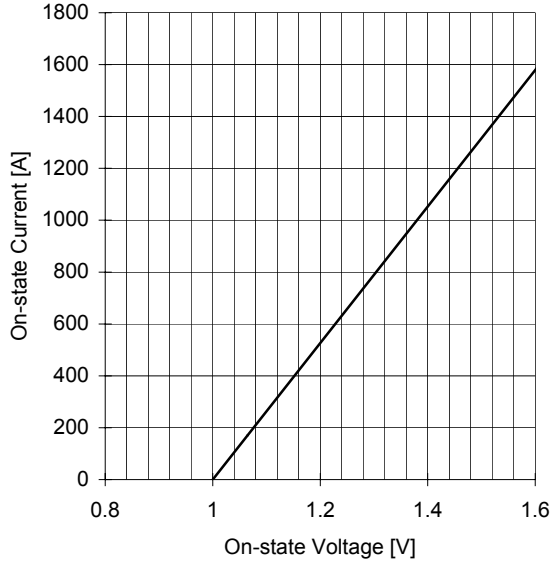
P_{F(AV)} [W]



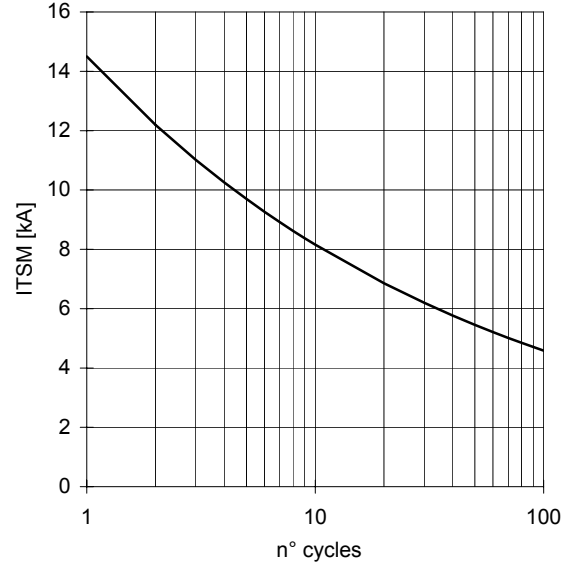
ATD571, ADT571 PHASE CONTROL MODULE

FINAL SPECIFICATION mar 01 - ISSUE : 01

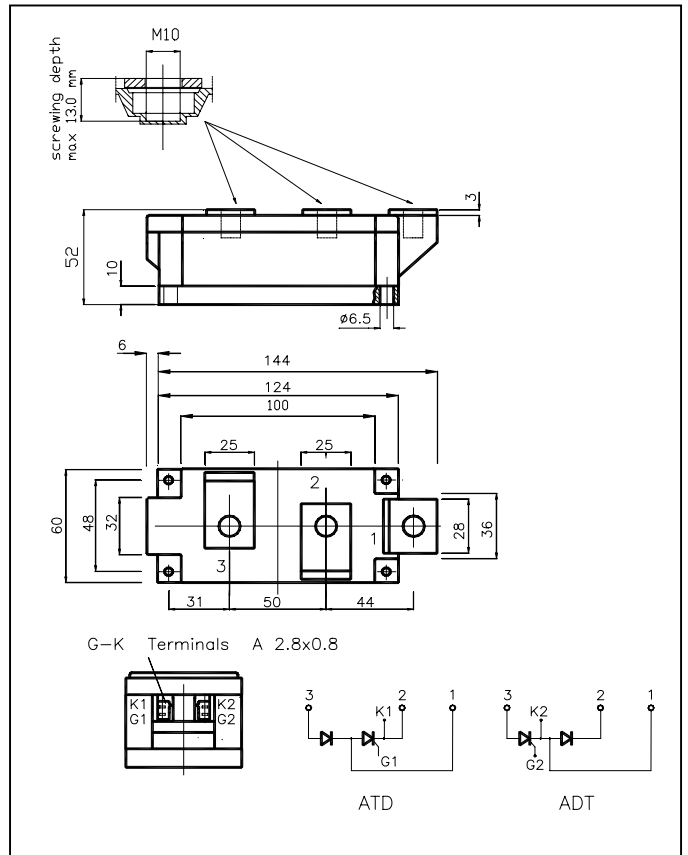
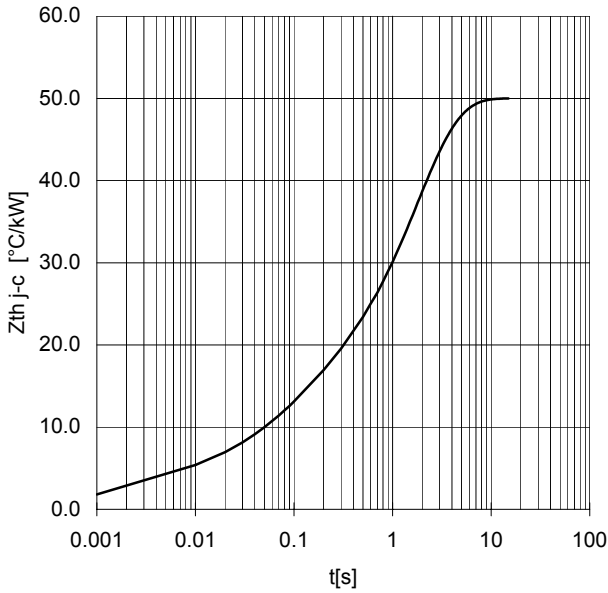
ON-STATE CHARACTERISTIC
 $T_j = 135^\circ\text{C}$



SURGE CHARACTERISTIC
 $T_j = 135^\circ\text{C}$



TRANSIENT THERMAL IMPEDANCE



All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness $< .03\text{ mm}$ and roughness $< 2\ \mu\text{m}$.

In the interest of product improvement POSEICO SPA reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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